

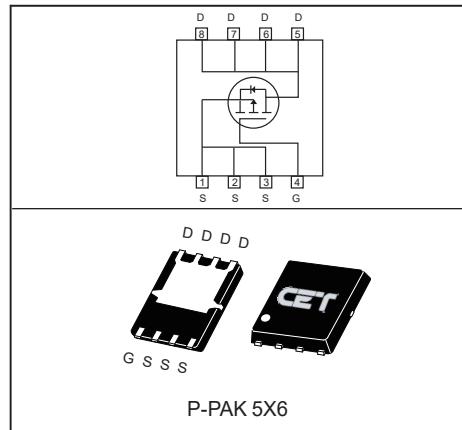
**P-Channel Enhancement Mode Field Effect Transistor****FEATURES**

- High power and current handing capability.
- Reliable and rugged.
- Pb-free lead plating ; RoHS compliant.
- Halogen Free.
- Surface mount Package.

**APPLICATIONS**

- DC/DC Converter.
- Power Management.
- Load Switch.

$V_{DSS}$	$R_{DS(ON)\text{ typ}} @ V_{GS}$	$I_D$
-60V	12m $\Omega$ @ $V_{GS} = 10V$	-40A

**ABSOLUTE MAXIMUM RATINGS**  $T_C = 25^\circ\text{C}$  unless otherwise noted

Parameter	Symbol	Limit	Units
Drain-Source Voltage	$V_{DS}$	-60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D @ R_{\theta JC}$	$T_C = 25^\circ\text{C}$	A
		$T_C = 70^\circ\text{C}$	A
	$I_D @ R_{\theta JA}$	$T_A = 25^\circ\text{C}$	A
		$T_A = 70^\circ\text{C}$	A
Drain Current-Pulsed <sup>a</sup>	$I_{DM} @ R_{\theta JC}$	$T_C = 25^\circ\text{C}$	A
	$I_{DM} @ R_{\theta JA}$	$T_A = 25^\circ\text{C}$	A
Maximum Power Dissipation	$P_D$	43	W
Single Pulsed Avalanche Energy <sup>d</sup>	$E_{AS}$	144.5	mJ
Single Pulsed Avalanche Current <sup>d</sup>	$I_{AS}$	17	A
Operating and Store Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$

**Thermal Characteristics**

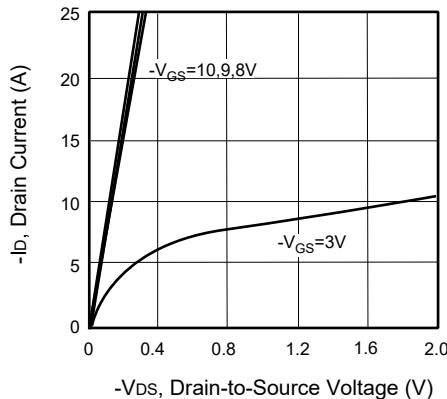
Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.9	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	20	$^\circ\text{C}/\text{W}$



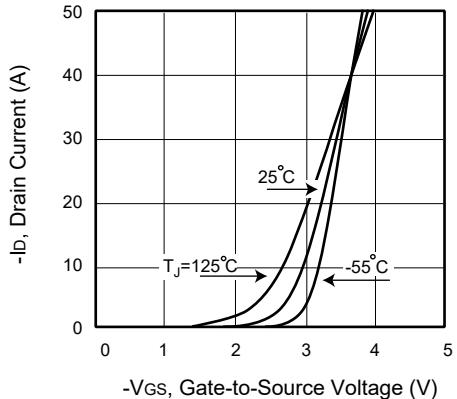
CEZ6145

**Electrical Characteristics**  $T_C = 25^\circ\text{C}$  unless otherwise noted

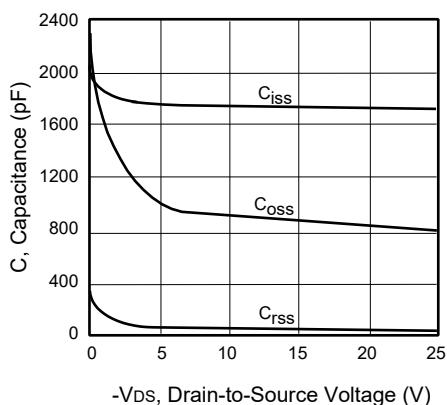
Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$\text{BV}_{\text{DSS}}$	$V_{\text{GS}} = 0\text{V}, I_D = -250\mu\text{A}$	-60			V
Zero Gate Voltage Drain Current	$I_{\text{DSS}}$	$V_{\text{DS}} = -60\text{V}, V_{\text{GS}} = 0\text{V}$			-1	$\mu\text{A}$
Gate Body Leakage Current, Forward	$I_{\text{GSSF}}$	$V_{\text{GS}} = 20\text{V}, V_{\text{DS}} = 0\text{V}$			100	nA
Gate Body Leakage Current, Reverse	$I_{\text{GSSR}}$	$V_{\text{GS}} = -20\text{V}, V_{\text{DS}} = 0\text{V}$			-100	nA
<b>On Characteristics<sup>b</sup></b>						
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{GS}} = V_{\text{DS}}, I_D = -250\mu\text{A}$	-1		-3	V
Static Drain-Source On-Resistance	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}} = -10\text{V}, I_D = -10\text{A}$		12	15	$\text{m}\Omega$
		$V_{\text{GS}} = -4.5\text{V}, I_D = -8\text{A}$		16	22	$\text{m}\Omega$
Gate Input Resistance	$R_g$	f=1MHz,open Drain		5.3		$\Omega$
<b>Dynamic Characteristics<sup>c</sup></b>						
Input Capacitance	$C_{\text{iss}}$	$V_{\text{DS}} = -25\text{V}, V_{\text{GS}} = 0\text{V}, f = 1\text{MHz}$		1685		pF
Output Capacitance	$C_{\text{oss}}$			805		pF
Reverse Transfer Capacitance	$C_{\text{rss}}$			35		pF
<b>Switching Characteristics<sup>c</sup></b>						
Turn-On Delay Time	$t_{\text{d}(\text{on})}$	$V_{\text{DD}} = -30\text{V}, I_D = -10\text{A}, V_{\text{GS}} = -10\text{V}, R_{\text{GEN}} = 6\Omega$		14		ns
Turn-On Rise Time	$t_r$			6		ns
Turn-Off Delay Time	$t_{\text{d}(\text{off})}$			44		ns
Turn-Off Fall Time	$t_f$			11		ns
Total Gate Charge	$Q_g$	$V_{\text{DS}} = -30\text{V}, I_D = -10\text{A}, V_{\text{GS}} = -4.5\text{V}$		14		nC
Gate-Source Charge	$Q_{\text{gs}}$			4		nC
Gate-Drain Charge	$Q_{\text{gd}}$			8		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
Drain-Source Diode Forward Current	$I_S$				-35	A
Drain-Source Diode Forward Voltage <sup>b</sup>	$V_{\text{SD}}$	$V_{\text{GS}} = 0\text{V}, I_S = -1\text{A}$			-1.2	V
<b>Notes :</b>						
a.Repetitive Rating : Pulse width limited by maximum junction temperature.						
b.Pulse Test : Pulse Width $\leq 300\mu\text{s}$ , Duty Cycle $\leq 2\%$ .						
c.Guaranteed by design, not subject to production testing.						
d.L = 1mH, $I_{\text{AS}} = 17\text{A}$ , $V_{\text{DD}} = 24\text{V}$ , $R_G = 25\Omega$ , Starting $T_J = 25^\circ\text{C}$ .						



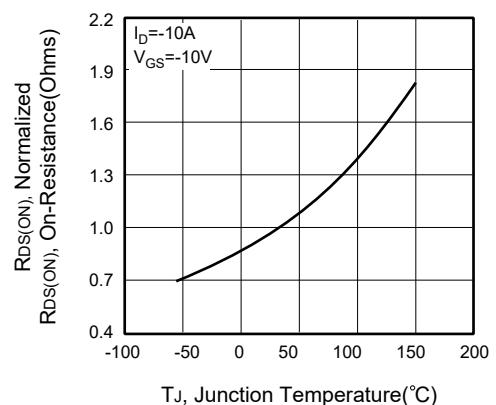
**Figure 1. Output Characteristics**



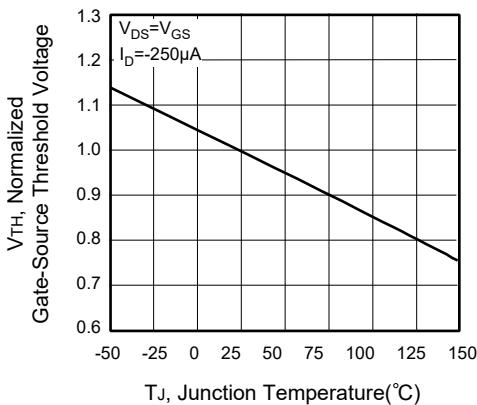
**Figure 2. Transfer Characteristics**



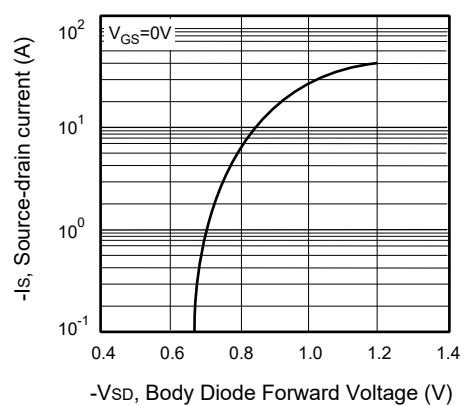
**Figure 3. Capacitance**



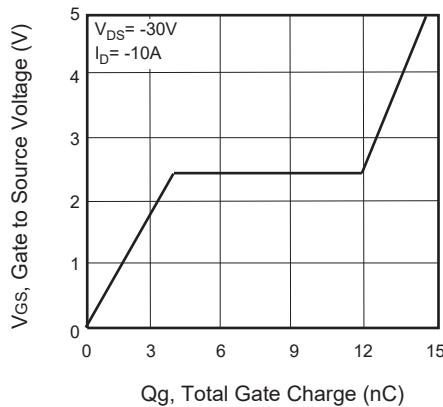
**Figure 4. On-Resistance Variation with Temperature**



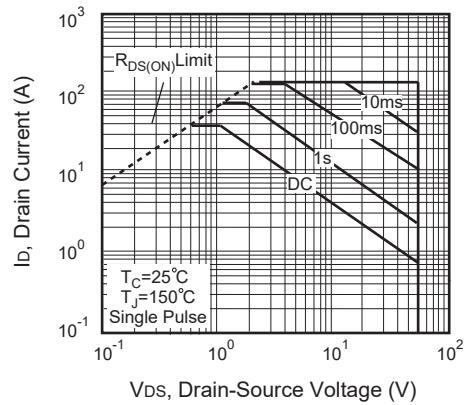
**Figure 5. Gate Threshold Variation with Temperature**



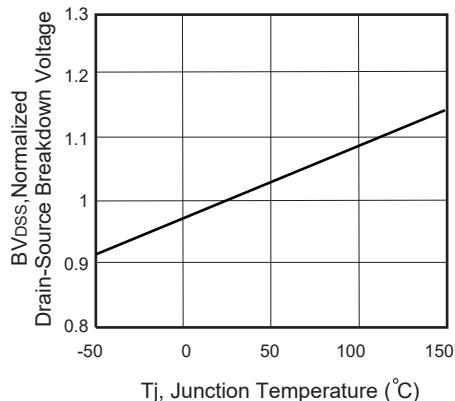
**Figure 6. Body Diode Forward Voltage Variation with Source Current**



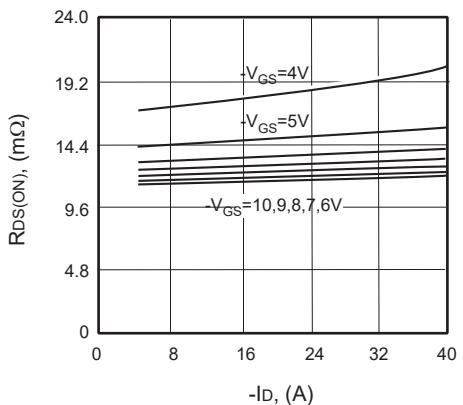
**Figure 7. Gate Charge**



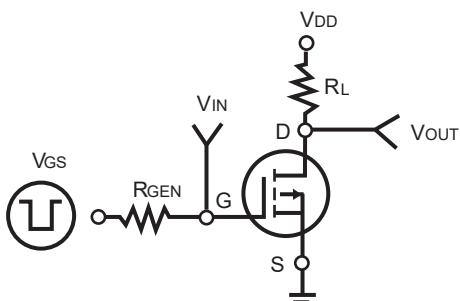
**Figure 8. Maximum Safe Operating Area**



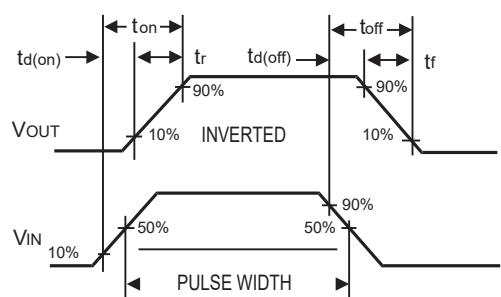
**Figure 9. Breakdown Voltage Variation VS Temperature**



**Figure 10. On-Resistance vs. Drain Current**



**Figure 11. Switching Test Circuit**



**Figure 12. Switching Waveforms**

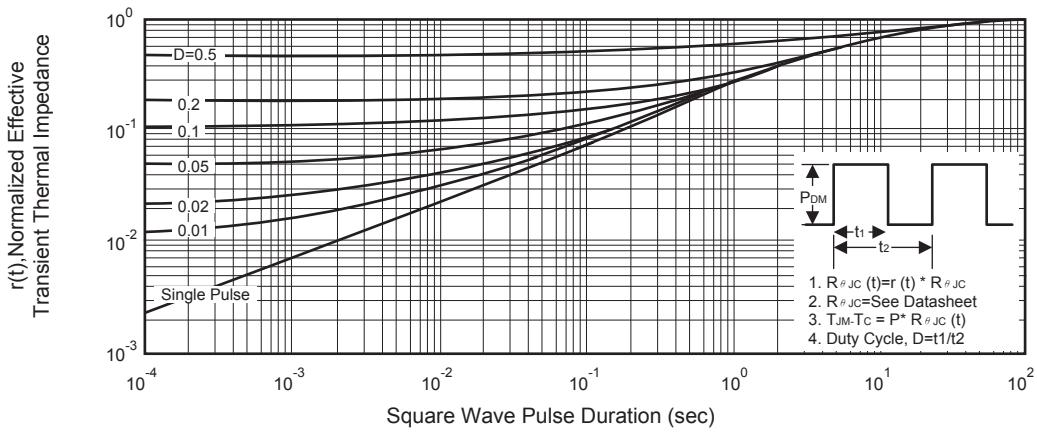
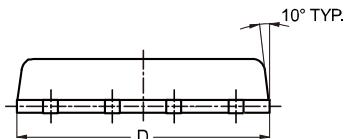
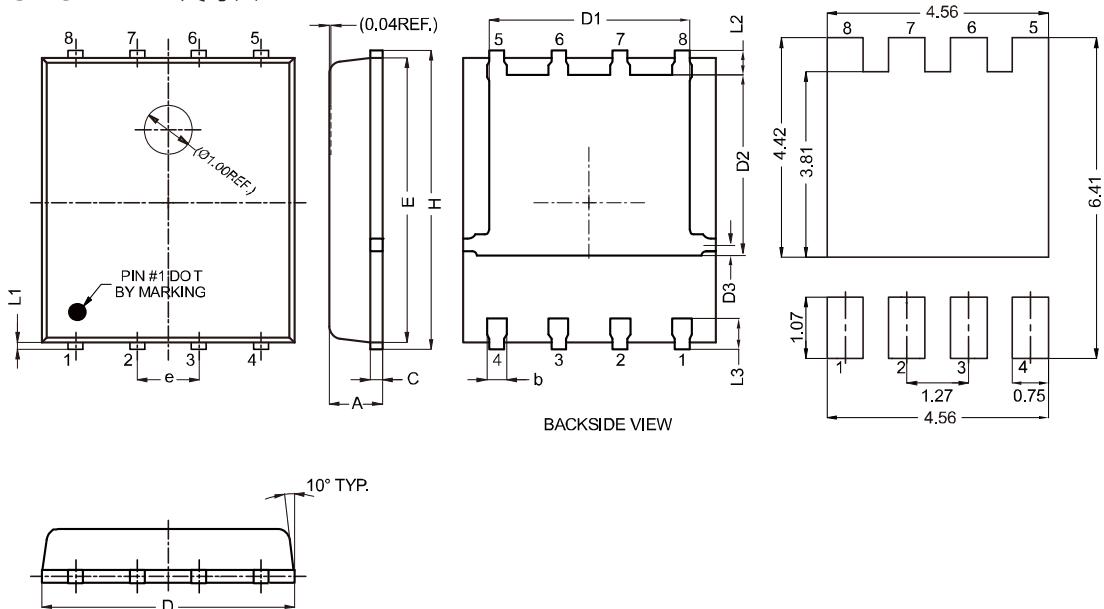


Figure 13. Normalized Thermal Transient Impedance Curve

**P-PAK5X6 產品外觀尺寸圖 (Product Outline Dimension)**
**SINGLE PAD 尺寸圖**

 Land Pattern  
 (Only for Reference)


SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.000	1.200	0.039	0.047
b	0.300	0.500	0.012	0.020
c	0.154	0.354	0.006	0.014
D	5.050	5.350	0.199	0.211
D1	3.800	4.250	0.150	0.167
D2	3.570	3.970	0.141	0.156
D3	0.380	0.850	0.015	0.033
E	5.660	6.060	0.223	0.239
e	1.270 TYP		0.050 TYP	
H	6.000	6.300	0.236	0.248
L1	0.080	0.330	0.003	0.013
L2	0.400	0.600	0.016	0.024
L3	0.500	0.700	0.020	0.028